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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* RICHARD DOUGLAS ALLAN and  
BERNARD JOSEPH CAMPBELL

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Appeal 2009-001167  
Application 09/696,099  
Technology Center 3600

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Decided: November 18, 2009

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*Before* MURRIEL E. CRAWFORD, HUBERT C. LORIN, and  
ANTON W. FETTING, *Administrative Patent Judges*.

LORIN, *Administrative Patent Judge*.

DECISION ON APPEAL

## STATEMENT OF THE CASE

Richard Douglas Allan et al. (Appellants) seek our review under 35 U.S.C. § 134 of the final rejection of claims 1-25. We have jurisdiction under 35 U.S.C. § 6(b) (2002).

## SUMMARY OF DECISION

We AFFIRM-IN-PART<sup>1</sup> and enter a new ground of rejection pursuant to 37 C.F.R. § 41.50(b).

## THE INVENTION

This invention is a transaction system that includes a plurality of transaction units which can include a coin validator, a banknote validator, a card reader, and a vending machine. Specification 1:19-22. “A single controller, which may be housed in one of the transaction units, is capable of controlling all the interconnected units. To achieve this, the controller has an operating system and a memory storing several units of executable code.” Specification 1:22 – 2:3.

Claim 1, reproduced below, is illustrative of the subject matter on appeal.

1. A value transaction system comprising a plurality of transaction units and a controller having a processor and memory means, the controller being operable to upload from said

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<sup>1</sup> Our decision will make reference to the Appellants’ Appeal Brief (“App. Br.,” filed Oct. 31, 2007) and Reply Brief (“Reply Br.,” filed Apr. 2, 2008), and the Examiner’s Answer (“Answer,” mailed Feb. 5, 2008).

transaction units respective run-time interpreted code units for storing in said memory means, the controller being operable to execute the code of each respective code unit and in response thereto to generate signals controlling the operation of the respective transaction units.

### THE REJECTIONS

The Examiner relies upon the following as evidence of unpatentability:

Coutts	US 6,311,165 B1	Oct. 30, 2001
Korman	US 6,318,536 B1	Nov. 20, 2001
Soltesz	US 2001/0011680 A1	Aug. 9, 2001

The following rejections are before us for review:

1. Claims 1-6 and 14-25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Coutts and Soltesz.
2. Claims 7-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Coutts and Korman.

### ISSUES

Would one of ordinary skill in the art have been led by Coutts and Soltesz to an apparatus having a controller that is operable to upload from the transaction unit's respective run-time interpreted code unit for storing in the memory means as recited in claims 1 and 14?

Would one of ordinary skill in the art have been led by Coutts and Korman to an apparatus having a validation transaction unit which has a validator component and a microprocessor system that includes at least one Java application operable to perform controlling functions for a further

transaction unit to which the validation unit is connected as recited in claim 7?

Would one of ordinary skill in the art have been led to Coutts and Soltesz to a method including a step of separately loading the executable code for the respective code modules from the associated transaction unit into the memory means of the controller as recited in claim 25?

## FINDINGS OF FACT

We find that the following enumerated findings of fact (FF) are supported by at least a preponderance of the evidence. *Ethicon, Inc. v. Quigg*, 849 F.2d 1422, 1427 (Fed. Cir. 1988) (explaining the general evidentiary standard for proceedings before the Office).

### *Claim construction*

1. The Specification states

In the following, the term “unit” is used to refer not only to a hardware device - that is, a transaction unit - preferably forming a discrete but connected part of the system, but also to a collection of software routines - that is, a code unit - which may, for example, control such a hardware unit.

Specification 2:3-6.

2. Claim 1 recites “the controller being operable to upload from said transaction units respective run-time interpreted code units for storing in said memory means.”

3. The Specification describes that the controller 16 is part of the coin changer 4, which is connected to the transaction units by an interface 14 in the controller and a Universal Serial Bus (USB) 12. Fig. 1 and Specification 4:13-15
4. The Specification states “[t]he contents of the memory in each unit are uploaded to the system controller 16 in an initialisation operation for that unit.” Specification 11:13-14.

*The scope and content of the prior art*

Coutts

5. Coutts describes an ATM, containing a number of peripheral devices, such as a card reader, receipt printer, and cash dispenser. Col. 14, l. 66 – col. 15, l. 2 and Fig. 8.
6. Coutts describes the ATM having a central processor connected to the peripheral devices through a RS-232 ink 136 (col. 15, ll. 5-7) or a universal serial bus (col. 19, ll. 64-67).
7. Coutts describes that device drivers and control applications are loaded into the central processor from a mass storage device when power is applied to the ATM. Col. 15, ll. 13-17.
8. Coutts describes the device drivers and control application independently running on the central processor to control the peripheral device. Col. 15, ll. 15-18.
9. Coutts describes an alternate embodiment having no central process, where the peripheral devices download software directly from a server. Col. 18, ll. 36-47 and Fig. 11.

10. Coutts describes a peripheral device containing a processor, a communications system and hardware control electronics. Col. 8, ll. 30-51 and Fig. 1.

Soltesz

11. Soltesz describes a self service kiosk. Soltesz [0003].
12. Soltesz teaches connecting the kiosk to the Internet to upload and download software. Soltesz [0034].

Korman

13. The Examiner cited Korman to teach that currency validation is known. Answer 4.

*Any differences between the claimed subject matter and the prior art*

14. Coutts does not describe that code units are uploaded from the transaction units.
15. Soltesz does not describe uploading code units from transaction units.
16. Coutts fails to teach a validation transaction unit which has a validator components and a microprocessor system that includes at least one Java application operable to perform controlling functions for a respective further transaction unit to which the validation unit is connected.

*The level of skill in the art*

17. Neither the Examiner nor the Appellants have addressed the level of ordinary skill in the pertinent art of value transaction systems. We will therefore consider the cited prior art as representative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (“[T]he absence of specific

findings on the level of skill in the art does not give rise to reversible error ‘where the prior art itself reflects an appropriate level and a need for testimony is not shown’”) (Quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

*Secondary considerations*

18. There is no evidence on record of secondary considerations of non-obviousness for our consideration.

## PRINCIPLES OF LAW

*Claim Construction*

During examination of a patent application, a pending claim is given the broadest reasonable construction consistent with the specification and should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

[W]e look to the specification to see if it provides a definition for claim terms, but otherwise apply a broad interpretation. As this court has discussed, this methodology produces claims with only justifiable breadth. *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed.Cir.1984). Further, as applicants may amend claims to narrow their scope, a broad construction during prosecution creates no unfairness to the applicant or patentee. *Am. Acad.*, 367 F.3d at 1364.

*In re ICON Health and Fitness, Inc.*, 496 F.3d 1374, 1379 (Fed. Cir. 2007).

Limitations appearing in the specification but not recited in the claim are not

read into the claim. *E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369 (Fed. Cir. 2003).

*Obviousness*

Section 103 forbids issuance of a patent when ‘the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [Graham] factors continue to define the inquiry that controls.”) The Court in *Graham* further noted that evidence of secondary considerations “might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.” *Graham*, 383 U.S. at 17-18.

## ANALYSIS

*The rejection of claims 1-6 and 14-25 under § 35 U.S.C. §103(a) as being unpatentable over Coutts and Soltész.*

*Claims 1-6*

The Appellants argued claims 1-6 as a group (App. Br. 6). We select claim 1 as the representative claim for this group, and the remaining claims 2-6 stand or fall with claim 1. 37 C.F.R. § 41.37(c)(1)(vii) (2009).

The Appellants argue that the combination of Coutts and Soltesz does not teach a controller uploading code *from a transaction unit* and using the code to control the *same transaction unit*, because Coutts describes downloading the software from a central server (App. Br. 6) and Soltesz describes downloading or uploading software from the Internet (App. Br. 7). *See* App. Br. 6-7 and Reply Br. 1-3. The Appellants argument is centered on the function of the claimed controller.

However, claim 1 recites an apparatus which includes a “controller being operable to upload from said transaction units respective run-time interpreted code units for storing in said memory means.” This limitation is drawn to the structure of the controller and not to the function steps performed by the controller. *Cf. In re Schreiber*, 128 F.3d 1473, 1477-78 (Fed. Cir. 1997) (functional language does not confer patentability if prior art structure has capability of functioning in the same manner). Claim 1 requires the controller to have *a structure that is capable* of being operated to upload code from said transaction units. We note that the Specification describes this structure broadly as controller 16 having an interface 14 that is connected to a Universal Serial Bus 12. FF 3-9. Giving this limitation the broadest reasonable construction in light of the Specification, we find that that this limitation encompasses a controller that has an interface and a connection. Coutts describes a central processor connected to peripheral devices through a Universal Serial Bus and the central processor controlling

the peripheral devices. FF 6. Therefore, we find that Coutts description teaches a controller having an interface and connection as required by the claim. Accordingly, we find that the Appellants have not shown that the Examiner erred in rejecting claim 1, and claims 2-6 dependent thereon, under 35 U.S.C. § 103(a) as unpatentable over Coutts and Soltesz.

*Claim 14-21*

The Appellants argued claims 14-21 as a group (App. Br. 8-9). We select claim 1 as the representative claim for this group, and the remaining claims 15-21 stand or fall with claim 14. 37 C.F.R. § 41.37(c)(1)(vii) (2009).

Like claim 1, claim 14 recites a “controller being operable to upload from each said transaction unit a respective code module containing executable code associated with that transaction unit for storage in said memory means.” The Appellants traverse the rejection of claim 14 for the same reasons as used to traverse the rejection of claim 1. App. Br. 8-9. Accordingly for the same reasons as discussed above with regards to claim 1, we find that the Appellants have not shown that the Examiner erred in rejecting claim 14, and claims 15-21 dependent thereon, under 35 U.S.C. § 103(a) as unpatentable over Coutts and Soltesz.

*Claim 22-24*

As further explained below, we will enter a new ground of rejection on claims 22-24 under 35 U.S.C. § 112, second paragraph, and reverse the rejection of claims 22-24 under 35 U.S.C. § 103(a) because it is necessarily based on speculative assumption as to the meaning of claim 22. *See In re*

*Steele*, 305 F.2d 859, 862-63 (CCPA 1962). Therefore, the prior art rejection must fall. Accordingly, the rejection of claims 22-24 under 35 U.S.C. § 103(a) is reversed.

*Claim 25*

Unlike the other independent claims, claim 25 is directed to a method having the step of “separately loading the executable code for the respective code modules from the associated transaction unit into the memory means of the controller.” This step is drawn to an action and not to the structure of the claimed controller as in the other independent claims.

We find that the Examiner has failed to establish a *prima facie* showing that one of ordinary skill in the art would have been led by the combination of Coutts and Soltesz to the claimed step. The Examiner relies upon paragraph [0034] Soltesz to teach this step and states, “Soltesz teaches method and corresponding system for . . . and separately loading executable code for the respective code modules from the associated transaction unit into the memory means of the controller (p3, 34).” Answer 3-4. However, we find that paragraph 34 of Soltesz describes downloading or uploading software for a kiosk from the Internet. FF 12. While Soltesz’s description does teach uploading and downloading of software to a kiosk from the Internet, this does not teach the step of *separately* loading executable code for the respective code modules from the *associated transaction unit*. We note that the Examiner admits that Coutts does not describe this step. Answer 3. Coutts describes downloading the code for peripheral modules from a mass storage device or server upon initialization of a peripheral module. FF 7 and 9. The Examiner has provided no other explanation of

why one of ordinary skill in the art would have been led by the combination of Coutts and Soltesz to the claimed step, other than asserting that Soltesz teaches the claimed step. *See Answer 3-4.* We find that the Examiner has failed to establish a *prima facie* showing of obviousness.

Accordingly, we find that the Appellants have shown that the Examiner erred in rejecting claim 25 under 35 U.S.C. 103(a) as unpatentable over Coutts and Soltesz.

*The rejection of claims 7-13 under § 35 U.S.C. §103(a) as being unpatentable over Coutts and Korman.*

The Appellants argue that neither Coutts nor Korman teaches a microprocessor with a JAVA application operable to perform controlling functions for a further transaction unit and the microprocessor being operable to upload the Java application from the further transaction unit as recited in claim 7. App. Br. 8. The Examiner does not respond to this argument (*see Answer 4-5*), but does state that Coutts teaches all of the limitations of claim 7 except for a currency validator, which the Examiner states is found in Korman. Answer 4.

We find that Coutts fails to teach a validation transaction unit which has a validator components and a microprocessor system that includes at least one Java application operable to perform controlling functions for a respective *further* transaction unit to which the validation unit is connected. FF 16. While Coutts does teach a central processor that has control applications that control multiple peripheral devices (FF 8), the central processor is not a validation transaction unit with validator components. Coutts also does not teach making a peripheral device control another

peripheral device, but instead describes the peripheral devices acting independently. FF 8. We note that the Examiner cited Korman for the general teaching that currency validators are known. FF 13. We find that Examiner has failed to establish a *prima facie* show of obviousness in rejecting claim 7. Accordingly, we find that the Appellants have shown that the Examiner erred in rejecting claim 7, and claims 8-13 dependent thereon, under 35 U.S.C. 103(a) as unpatentable over Coutts and Korman.

#### NEW GROUND OF REJECTION

Pursuant 37 C.F.R. § 41.50(b), we enter a new ground of rejection on claims 22-24 under 35 U.S.C. 112, 2<sup>nd</sup> paragraph.

Claim 22 recites a means-plus-function limitation. Claim 22 recites “at least one transaction unit including means for performing value transactions under the control of the processor executing code uploaded from the transaction unit.” A means-plus-function limitation is construed to cover the corresponding structure, materials, or acts described in the written description of the Specification and equivalents thereof. However, the Specification does not describe structure corresponding to this limitation.

We note that the Appellants, in the Appeal Brief, cite to page 6, lines 18-20 and page 11, lines 11-14 of the Specification as support for this limitation. From those passages, we find that the claimed transaction unit corresponds to transaction units 4, 6, 8, and 10 in the Specification and that the claimed code executed by the processor and uploaded from the transaction unit are modules 30, 32, and 34 in the Specification. However, we do not find the corresponding structure for the claimed *means for performing value transactions*, which is part of the transaction unit in these

passages or the remainder of the Specification. Therefore, we cannot construe the limitation and the claims are indefinite.

## CONCLUSIONS OF LAW

We conclude that the Appellants have not shown that the Examiner erred in rejecting claims 1-6 and 14-21 under 35 U.S.C. §103(a) as unpatentable over Coutts and Soltesz.

We conclude that the Appellants have shown that the Examiner erred in rejecting claims 22-24 and 25 under 35 U.S.C. §103(a) as unpatentable over Coutts and Soltesz and in rejecting claims 7-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Coutts and Korman.

A new ground of rejection has been applied to claims 22-24 under 35 U.S.C. § 112, second paragraph.

## DECISION

The decision of the Examiner to reject claims 1-24 is affirmed and to reject claims 7-13 and 22-25 is reversed. We enter a new ground of rejection on claims 22-24 under 35 U.S.C. 112, second paragraph.

This decision also contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides “[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.” This Decision contains a new rejection within the meaning of 37 C.F.R. § 41.50(b) (2007).

37 C.F.R. § 41.50(b) also provides that the appellants, **WITHIN TWO MONTHS FROM THE DATE OF THE DECISION**, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

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- (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner . . . .
- (2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same record . . . .

AFFIRMED-IN-PART; 37 C.F.R. § 41.50(b)

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